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Iwamatsu et al.

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[54] CLOCK PHASE DETECTING CIRCUIT AND
CLOCK REGENERATING CIRCUIT EACH
ARRANGED IN RECEIVING UNIT OF
MULTIPLEX RADIO EQUIPMENT

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375/344; 329/304

[58] Field of Search 375/279-281.
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307, 308

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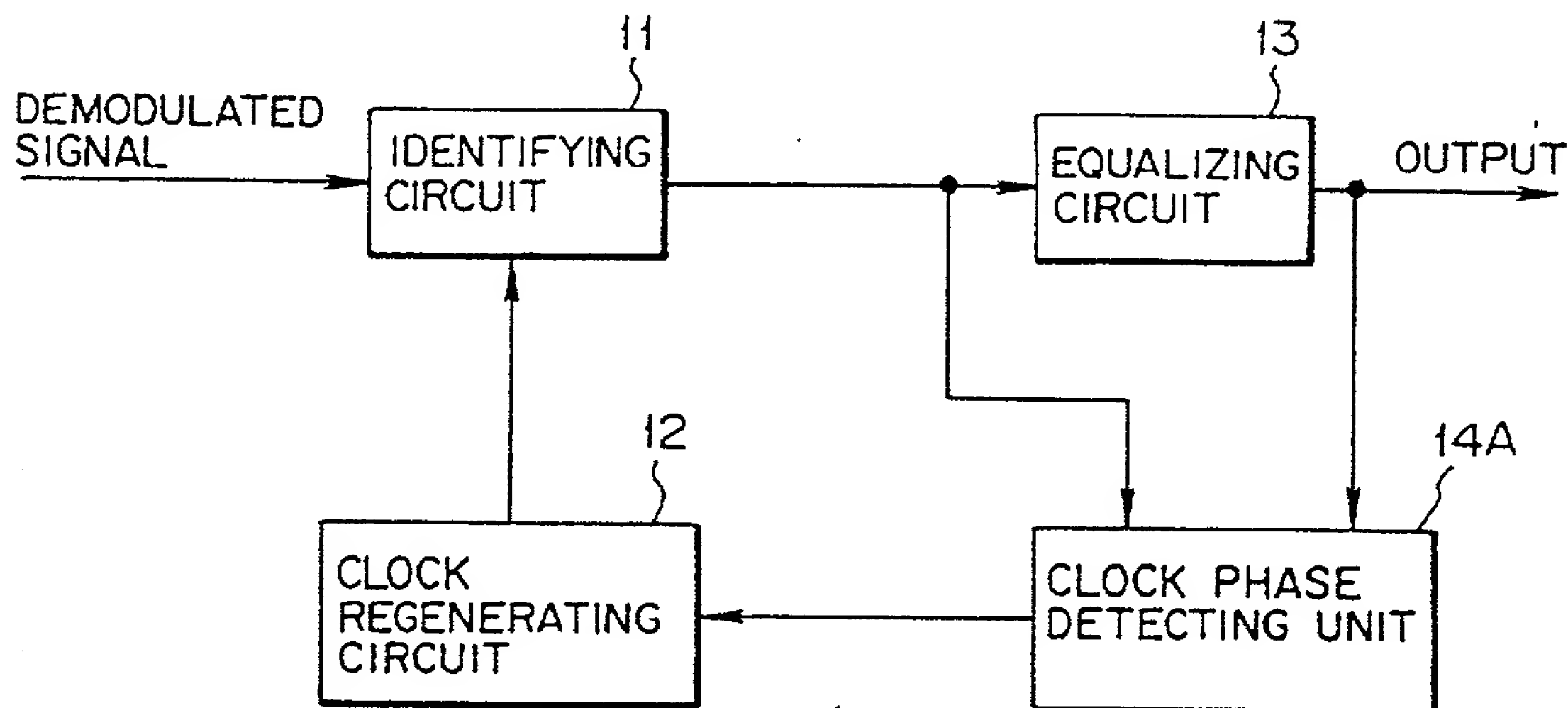
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[57] ABSTRACT

The present invention relates to a clock phase detecting circuit and a clock regenerating circuit each arranged in a receiving unit of multiplex radio equipment. The receiving unit of the multiplex radio equipment includes an identifying circuit for identifying a signal obtained by demodulating a multilevel orthogonal modulation signal; a clock regenerating circuit for regenerating a signal identification clock for the identifying circuit to supply the clock to the identifying circuit; an equalizing circuit for subjecting the signal obtained by demodulating a multilevel orthogonal modulation signal to an equalizing process. A clock phase detecting unit detects the phase component of the signal identification clock based on signals input to or output from the equalizing circuit and then supplies the phase component to the clock regenerating circuit. The phase component of a signal identification clock can be certainly detected and accurately adjusted so that the signal identification clock can be regenerated with high accuracy.

14 Claims, 61 Drawing Sheets



1A: CLOCK PHASE DETECTING CIRCUIT